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MONOLITHIC TELEMETRY FOR ACOUSTIC ARRAYS.(U)
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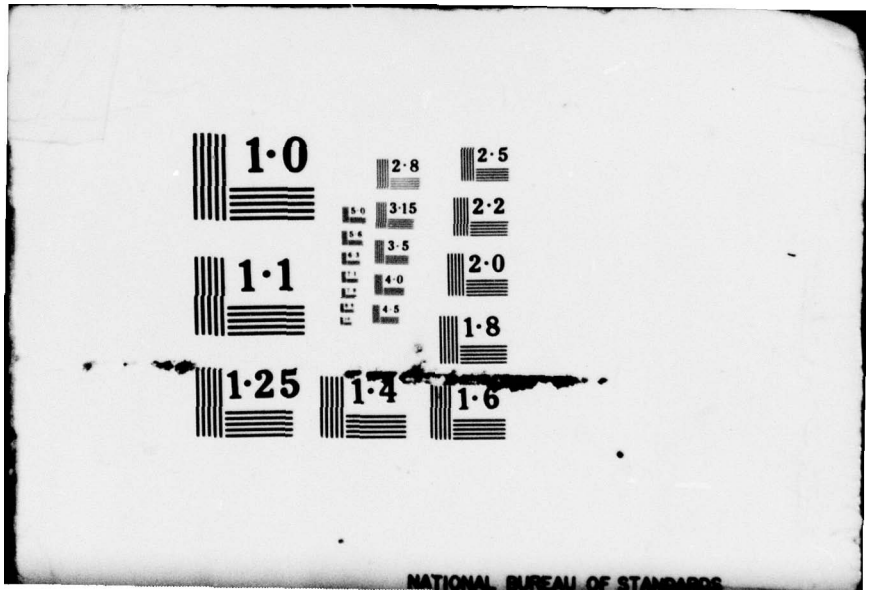
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LEVEL II

FINAL REPORT

MONOLITHIC TELEMETRY FOR ACOUSTIC ARRAYS

Contract N6604-6289-0811

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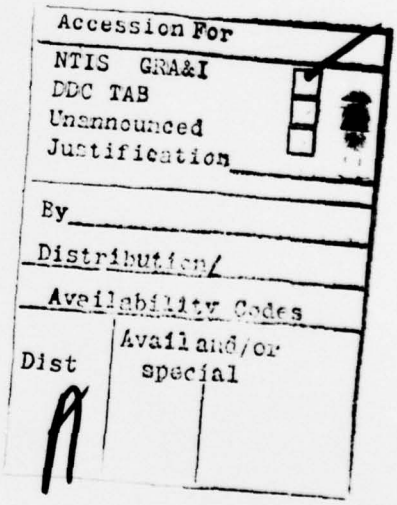

SUMMARY OF WORK

A design tradeoff study of a telemetry system has been conducted by Texas Instruments Incorporated over a time period from 5 November 1976 to 20 December 1977 for the Naval Underwater Systems Center (NUSC) for application to the Ranging Array using Thin Line Array technology. The study addressed electrical and mechanical interface requirements and considered commonality with other anticipated array developments. Personnel at Texas Instruments Incorporated participating in the design study were with the Anti-Submarine Warfare Department, the Custom Engineering Center, and the Advanced Engineering branch of the Equipment Group.

The overall objective of the Thin Line Array program at NUSC is to develop a high performance, reliable acoustic array at moderate cost which can be deployed from a submarine or a surface vessel with a minimum of handling equipment, and which will acquire data used to detect, classify, and locate adversary submarine activity. The objective of the subject program is to perform preliminary engineering tasks to validate concepts of telemetry functions for thin line-type arrays on monolithic chips. A subsequent program phase would develop an acoustic array telemetry unit in a standard module for the Thin Line Array. Utilization of the LSI technology will reduce per-channel unit cost, increase reliability, and decrease size relative to alternative approaches.

This study is performed as a system engineering task to insure that the telemetry configuration is compatible with the overall system requirements and to provide interface and packaging information. The study results are intended to guide the actual design and breadboarding of signal conditioning and digital multiplexer functions of the telemetry unit. It is anticipated that the development effort will continue to involve tradeoffs of performance and costs, and that Texas Instruments will maintain close liason with NUSC in resolving those tradeoffs.

The study involved telephone contact, correspondence, and meetings with personnel from New London Laboratory, NUSC. A literature search was conducted

on subjects of pressure tolerant electronics, array telemetry requirements, data conversion and encoding, and active filter design. This report includes a summary of array requirements in Section 1 and recommendations for telemetry unit design for Section 2. The telemetry unit technical description presented in the proposal for this program is still a valid model, with variations and additional particulars as set forth in the following sections.

1. Array Requirements

The Ranging Array telemetry requirements which were determined are set forth in the following paragraphs. Telemetry system specifications of the wide aperature hull mounted array, SURTASS, and SQR-19 (ETAS) acoustic arrays were reviewed for commonality of requirements with the subject array. The telemetry system under study presents a good potential for lower cost, higher reliability, and performance equivalence to any of these other applications. The lower cost would be a result of minimal array interconnect wiring and low telemetry unit cost because of LSI electronic technology and pressure tolerant electronics packaging. The higher reliability is also due to minimal array interconnects and LSI electronics. The requirements for signal conditioning and processing performance need be extended only for higher bandwidth and greater dynamic range to meet the overall system requirements of all other arrays studied. The signal bandwidth can be extended by changing filter component values and increasing the sample rate. Dynamic range can be increased by optimizing the data encoding technique and increasing the number of bits allocated to each sample. The custom digital circuit will be designed with several features providing flexibility for adaption to other array applications. The analog circuit design parameters can be further improved by component selection and acceptance testing and will continue to be a cost/performance tradeoff.

1.1 Array Data Performance.

The following parameters reflect the performance required for the Ranging Array.

1.1.1 Number of channels.

The acoustic array must accomodate as many as 256 channels.

1.1.2 Signal bandwidth. The pass band is from 10 Hz to 1000 Hz with a +6 dB/octave response high-pass slope referenced to the hydrophone signal present at the pre-amplifier input.

1.1.3 Dynamic range. Wideband dynamic range will be 70dB. This provides for logarithmic data encoding onto a sign bit and seven binary data bits with a resolution of 1/2 dB/bit.

1.1.4 Harmonic distortion. Limited to 3% maximum.

1.1.5 Channel/channel response. Channel/channel gain variation will be within $\pm$ 1/2 dB and channel/channel phase within $\pm 2^{o}$.

1.1.6 System noise. -10 dB referenced to Sea State 0 which is:

- 120 dBV/Hz at 10 Hz
- 140 dBV/Hz at 100 Hz
- 160 dBV/Hz at 1000 Hz

1.1.7 Calibration. The goals of calibration (in order of importance) will be:

- Detect individual unit failures
- Determine relative unit gain and phase at a single frequency
- Determine relative unit gain and phase over frequency band.

If all the calibration goals can be met, correction parameters can be applied to digital processing to cancel any unit gain and phase variations. A signal will be injected in series with the hydrophone at the pre-amplifier. The signal will be a rectangular wave which is counted down from the channel sample rate and phased to the beginning of a calibration so that channel/channel excitation will be coherent. An accurate amplitude reference and sharp signal switching will be important for good calibration results.

1.2 Telemetry Unit Electrical Interface

1.2.1 Hydrophone parameters

Sensitivity = - 195 dBV/μP

Capacitance = 2 to 3 kpf

Input Impedance = 40 megohms

1.2.2 Power consumption. A goal has been set at less than 1/2 watt per channel.

1.2.3 Master clock input. The clock will be a 6 MHz bipolar signal at 2 V p-p transmitted over 50 ohm coaxial cable. The shield will have up to 130 V dc potential and must be ac coupled. The signal line must also be ac coupled. The word, frame, and calibration commands are transmitted as one, two, or three consecutive double amplitude pulses respectively. The telemetry unit must detect the clock and commands over a range of at least 24 dB (attenuation of 1200 feet of cable).

1.2.4 Data output. The array telemetry format will be time-division multiplexed as shown in Figure 1-1. The telemetry units will each output one encoded data value per frame. Each unit will transmit eight bits of data in the time slot corresponding to its channel address. A "one" bit will be represented by a pulse and a "zero" bit will not present a pulse to the signal line. Each unit will transmit "one" bit pulses in a bipolar format to avoid dc "wander". The amplitude of the data output is established by the clock level detection. Clock and data should be equally attenuated by their coaxial cables, and thus the entire data bit stream at the end of the array should be at a normalized amplitude.

1.2.5 Programming inputs. Terminals or contacts shall be externally accessible at each telemetry unit, so that channel address and other parameters may be set before the unit is installed in the array.

1.3 Telemetry Unit Mechanical Interface

1.3.1 Number of channels. As many as 256 channels must be accomodated. Universal sparing of telemetry units will reduce logistics costs.

1.3.2 Size. The telemetry units must fit into an array with an inside diameter of 3/8". The unit must be under 3" in length.

1.3.3 Environment. The units will be immersed in oil or solid foam with up to 2000 psi pressure and a temperature range of $+35^{o}C$ to $-5^{o}C$.

1.3.4 Array wiring. The number of array interconnects will be kept to a minimum to increase relability and lower system costs. Array length may be 1200 feet or more, with clock and data transmission by coaxial cables. Also, all array wiring including interconnects must be contained in a diameter of 3/8".

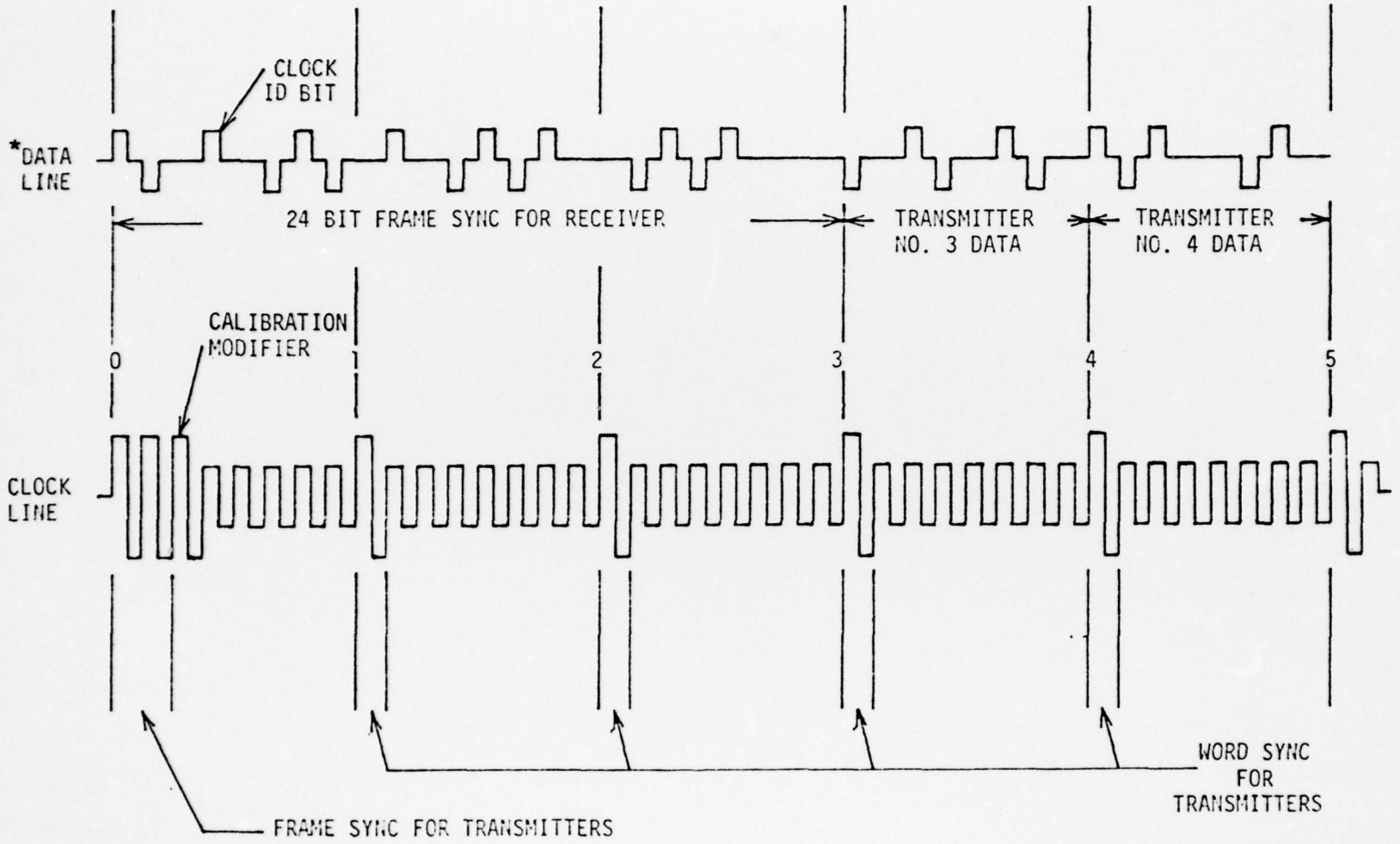

Figure 1-1 Waveforms of Data and Clock Lines

*NOTE: There will be an inherent 2 bit time delay of data from all transmitters which is omitted here for clarity.

2. Telemetry Unit Implementation

2.1 Electronic Design. The telemetry unit block diagram is shown in Figure 2-1. Possible modifications are discussed in the following paragraphs.

2.1.1 Telemetry Format. Array data is digitally encoded, modulated, and transmitted in a time-division multiplex format shown in Figure 1-1. The modulation used is "bipolar", with each unit transmitting alternative positive and negative pulses to represent "one" data bits. Only a single unit transmits at any time, and the output of each unit is in no way conditioned by the outputs of other units. The nominal word length will be eight bits, with the most significant (sign) bit transmitted first. A provision to transmit bit lengths of nine or ten is being considered in the digital LSI chip for expansion capability.

2.1.2 Clock receiver and detector. The differential clock receiver will be ac coupled to the clock signal to block dc offset voltages. Each unit must detect the double amplitude command and timing information. The clock signal will be attenuated along the array at about 2 dB/100 feet. The detector circuit will amplify and square the clock to provide timing for the telemetry unit. The differential signal will also be tracked by a synchronous detector. The filtered output from the detector will detect double amplitude clock pulses and establish a relative drive level for the line driver output.

2.1.3 Data line driver. The data line driver output and return will be ac coupled to the line to block dc offset voltages. The output stage drive is referenced to the synchronous detector and must sink and source up to 40 milliamp into the 50 ohm line. The output stage will have series attenuation so that a failure in one unit will not render the array inoperable. The driver output conditions are current source, open, and current sink. The open condition is present when the unit is not enabled or when the data is a "zero". The current source and current sink conditions are alternately present to transmit "one" bits.

2.1.4 Signal conditioning. The major signal conditioning elements are shown functionally as a pre-amplifier, filter, logarithmic amplifier, and track and hold circuits. The signal conditioning electronics must meet

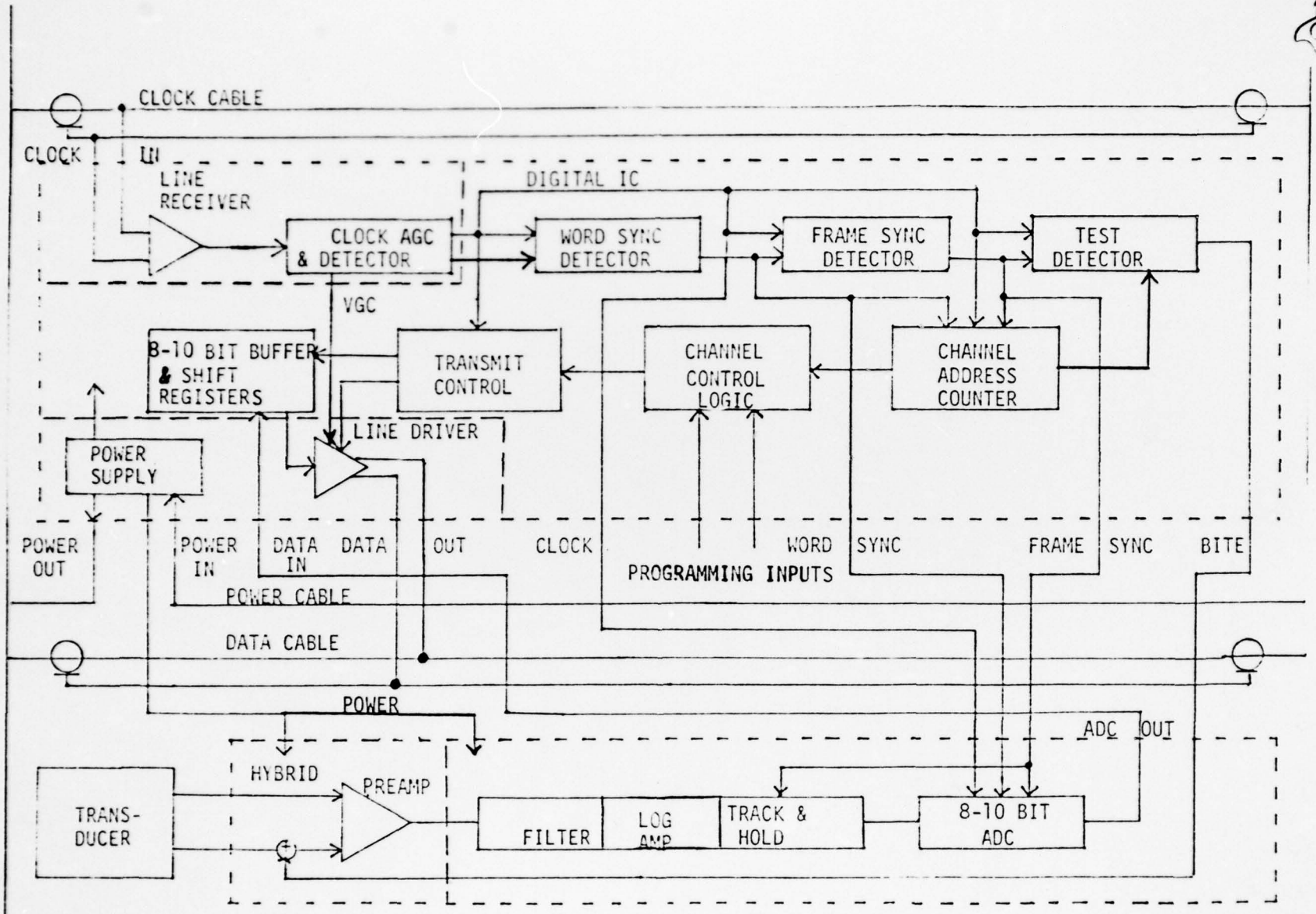

Figure 2-1 Telemetry Block Diagram Unit

stringent array data requirements as stated in Section 1.1. The implementation and partitioning of this section is critical to the overall unit performance.

2.1.4.1 Pre-amplifier. The pre-amplifier will present a 40 megohm resistive load to the hydrophone. A field-effect transistor (FET) input stage will be used to obtain high impedance and low current noise. A differential input configuration will be used to avoid drift and the need for adjustment, using matched FET's. Provision will be made for injecting a calibration signal in series with the hydrophone. An operational amplifier stage will provide passband pre-emphasis and most of the pre-amplifier gain.

2.1.4.2 Filter. Low frequency rolloff will be incorporated in the filter section to keep low frequency spectrum noise from saturating successive stages of the signal conditioning electronics. The filter section will provide some overall signal gain to the input of the log amplifier. The filter section will implement a low pass, four pole Butterworth with a corner frequency of 1 kHz (for Ranging Array application). This filter provides low passband ripple and 24 dB/octave attenuation of aliased frequencies caused by signal sampling and reconstruction. The filter section will be implemented so that successive stages can be "tuned" by resistor trimming before the telemetry unit assembly is complete.

2.1.4.3 Logarithmic amplifier. The signal samples must be compressed to provide maximum dynamic range while maintaining $\pm$ 1/2 dB in resolution with eight bits of data. The most efficient way to encode the data is with a logarithmic response. The log amplifier will perform the compression and allow use of a standard analog-to-digital converter design with a precision of only eight bits. There will be a sign bit, and bit weights of 32, 16, 8, 4, 2, 1, and .5 dB. Existing bipolar monolithic log amplifiers attain the 70 dB performance required and far exceed the tracking rates required. It is anticipated that an existing design will be modified to reduce power sonsumption, as a tradeoff against unnecessary speed. Temperature tracking problems are minimal because of the limited operational temperature range.

2.1.4.4 Track and hold. This function is required to maintain a constant input sample amplitude at the analog-to-digital converter while a conversion is taking place. The low sample rate (2928 per second) and data compression of the log amplifier combine to ease the performance requirements of the track and hold. This function may be combined with the log amplifier on a custom monolithic circuit.

2.1.5 Analog-to-digital converter. The conversion scheme selected is one of successive approximation and will probably use offset binary encoding. The major sections of the converter are an output register, resistor ladder network, comparator, and control/timing logic. The converter will provide a serial output and clocking to the custom digital IC. An attempt will be made to implement the converter with standard monolithic chips, but the timing/control logic may be incorporated into the custom digital IC. The converter will be designed to produce 10 bits of output, to be compatible with future system requirements and provide flexibility.

2.1.6 Digital control. The digital timing and control circuits will be implemented in a custom monolithic IC. The word, frame, and test detectors are simple logic circuits that look for one, two, or three successive double-amplitude synchronizing clocks. The test detector also contains a divider circuit which generates one or more rectangular waves from the data sample rate for system calibration. The 8-bit channel address counter resets on frame sync and increments on word sync with a count from 0 to 255. The channel control logic compares the channel address count to pre-programmed memory elements, and enables the transmit control when they are equal. Potentially, there will be other memory elements which can provide control for data rate, bit length, etc. The transmit control enables the line driver output stage, shifts data into and through a serial output register, and encodes "one" data bits as alternate level pulses. The buffer register receives serial data from the ADC. Data is parallel transferred from the buffer register to the output register at each frame sync. Output register data is shifted to the line driver when the unit's address is detected. Control/timing elements of the ADC may be implemented in the same chip if partitioning and circuit complexity favor that approach.

The digital IC may be implemented either in TTL or I^2L technology. I^2L implementation would result in lower power dissipation, but TTL is presently capable of higher speeds. Detailed logic design is essentially independent of the technology, in fact the number of gate levels of propagation delay between clocks will determine if I^2L technology can be used. The major consideration in detailed design of the chip is to incorporate flexibility of application by way of external programming and external wiring. The device complexity is estimated at from 400 to 700 logic gates.

2.1.7 Power Supply. The power distribution within the telemetry array will be series-parallel to minimize current requirements while keeping voltages within reasonable limits. Each unit will be supplied with 24 to 28 volts at some nominal current. The unit should incorporate a bypass circuit for overvoltage protection and to maintain constant current flow in case of failure within the power supply of that unit. A series regulation circuit to develop 20 volts ($\pm$10) will supply the analog circuit elements. Some output capacitance will be required to supply the high current line driver pulses. The digital IC will need 5 volts if TTL implementation is selected and 1.4 volts if I^2L is selected. In either case, the large stepdown voltage ratio will rule out a series regulator, due to very poor efficiency. The digital circuits may be "seriesed" or "stacked" with the analog elements in one or more sections. This approach would require level translation on any signals between analog and digital sections or between digital sub-sections. It is more probable that a switching regulator will be used to step the input voltage down to drive the digital circuits.

2.1.8 Partitioning. An optimum design for the digital IC is considered essential. The number of interface lines must be carefully controlled, while maintaining design flexibility. Each interface to the digital IC should also be simple and straightforward. The number of precision components will be kept to a minimum, because they require hybrid components, trimming, and chip connections. The pre-amplifier and filter sections will be implemented in hybrid form, using operational amplifier chips bonded to the hybrid substrate. IC chip carriers will probably be used, so that portions of the telemetry unit electronics can be individually tested to improve yield. The

log amplifier, sample and hold, analog-to-digital converter, clock detector, and line driver circuits will be implemented with a combination of standard and custom monolithic chips.

2.2 Packaging concepts. The two basic approaches to packaging the telemetry units are a pressure vessel cylinder and molded epoxy over pressure tolerant electronics. Pressure vessel technology is well-known, but involves higher tooling and manufacturing costs and presents sealing/penetration problems. A molded epoxy package, as illustrated in Figure 2-2, containing pressure tolerant electronics would reduce manufacturing costs and allow a good environmental interface (thermal conduction, vibrations, sealing). Documented knowledge and tests of LSI electronic chips in a high pressure environment is very limited, and thus a definite risk is involved in this approach. The packaging concept will have little effect on the detailed circuit design and partitioning of the electronics, and that work can proceed independently. Pressure tolerant electronics is the selected approach with a backup position of enclosing the electronics in a pressure vessel.

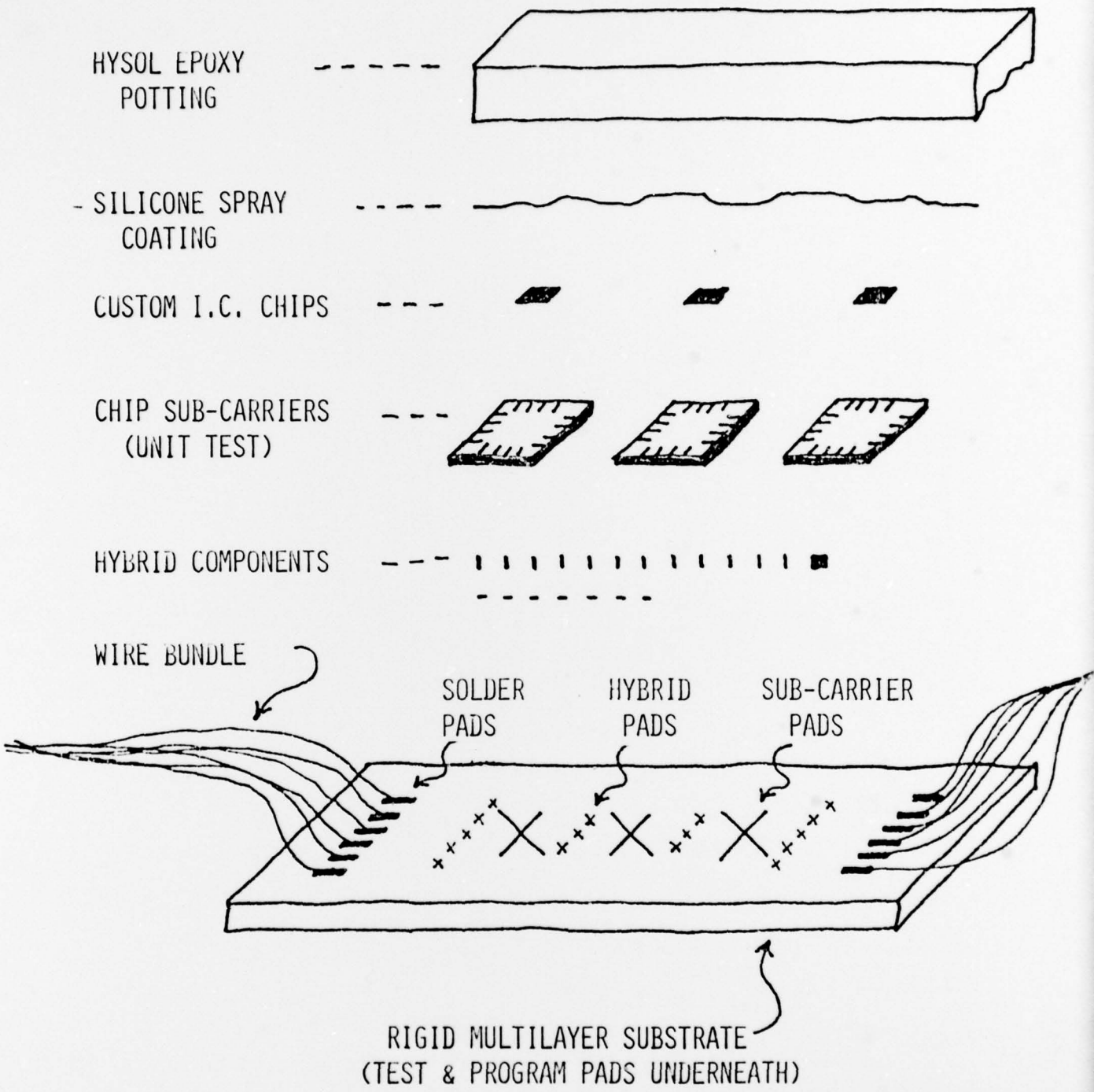

Figure 2-2. Telemetry Unit Packaging

CONCLUSIONS

This study concentrated on examination of electrical and mechanical interface requirements for the telemetry units in the thin line array. The proposed telemetry unit design was reviewed in light of these requirements. Recommendations for insuring a most effective design are:

(1) Implement the pre-amplifier and filter section in hybrid technology because precision components are involved and signal conditioning requirements are more subject to change.

(2) Encode the data efficiently as a logarithmic response. Implement the log amplifier as a metal-mask spin off of an existing product to reduce development costs.

(3) Implement a standard eight-bit, analog-to-digital converter and a track-and-hold circuit with minimal requirements because of the data compression in the log amplifier. Partitioning and implementation tradeoffs will have to be done in the detailed design phase.

(4) Implement the clock detector, line driver, and possibly the power supply and portions of the anlog-to-digital converter as a custom analog chip.

(5) Implement a custom digital chip with flexibility provided by external programming capability for unit address, bit length, and data rates.

(6) Use chip carriers and hybrid substrates to allow testing of individual circuits or sections of the telemetry unit electronics. This will reduce costs by raising overall yields on final assemblies.

(7) Use only electronic components that are believed to have pressure tolerance. This may affect the telemetry unit packaging costs. Similar telemetry unit electronics has been implemented for NUSC in hybrid form with pressure vessel packaging techniques. Design of custom digital and analog chips and use of pressure tolerant electronics will reduce telemetry unit cost, improve the data performance, and allow incorporation of flexibility to extend applications thereof.

(8) Final design decisions should be made during a breadboard phase where various semiconductor technologies are considered along with development and production costs. Generally more functions can be incorporated into a custom IC at the expense of greater development costs and risk. Thus, chip complexity involves a tradeoff between development costs and production costs. Increased chip complexity is ultimately limited by the acceptable production yield. Production quantities and yield result in a floor on per unit device costs. Economic factors will primarily determine the chips complexity and partitioning of the telemetry system.